Intrinsic Nonlinearities and Layout Impacts of 100 V Integrated Power MOSFETs in Partial SOI Process

Fan, Lin; Knott, Arnold; Jørgensen, Ivan Harald Holger

Publication date:
2016

Document Version
Publisher's PDF, also known as Version of record

Intrinsic Nonlinearities and Layout Impacts of 100 V Integrated Power MOSFETs in Partial SOI Process

Lin Fan, Arnold Knott, Ivan Harald Holger Jørgensen
Technical University of Denmark, Department of Electrical Engineering, Electronics Group
Richard Petersens Plads, Building 325, Room 258, 2800 Kgs. Lyngby, Denmark

Abstract

Parasitic capacitances of power semiconductors are a part of the key design parameters of state-of-the-art very high frequency (VHF) power supplies. In this poster, four 100 V integrated power MOSFETs with different layout structures are designed, implemented, and analyzed in a 0.18 µm partial Silicon-on-Insulator (SOI) process with a die area 2.31 mm^2.

A small-signal model of power MOSFETs is proposed to systematically analyze the nonlinear parasitic capacitances in different transistor states: off-state, sub-threshold region, and on-state in the linear region. 3D plots are used to summarize the intrinsic nonlinearities of the power devices. The nonlinear figure-of-merits (FOMs) are lowered by 1.3-18.3 times and improved by 22-95 % with optimized conditions of quasi-zero voltage switching. The layout impacts of the on-chip interconnections are analyzed with post-layout comparisons.

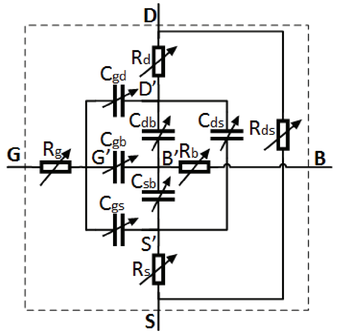


Figure 1. Proposed small-signal model of power MOSFETs (off-state, sub-threshold region, and on-state in the linear region)

Intrinsic Nonlinearities in Frequency-Domain

(Nonlinear Capacitances @ 1 MHz)

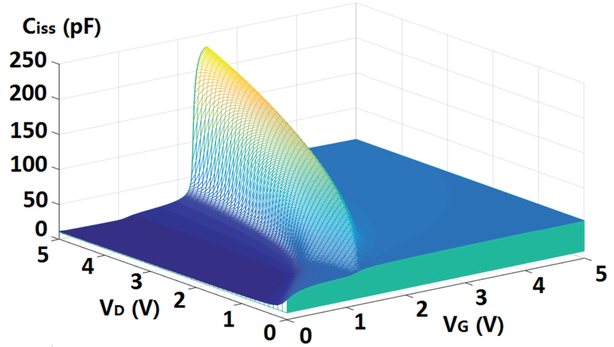


Figure 2. Nonlinearities of C_{iss} (off-state, sub-threshold region, and on-state in the linear region)

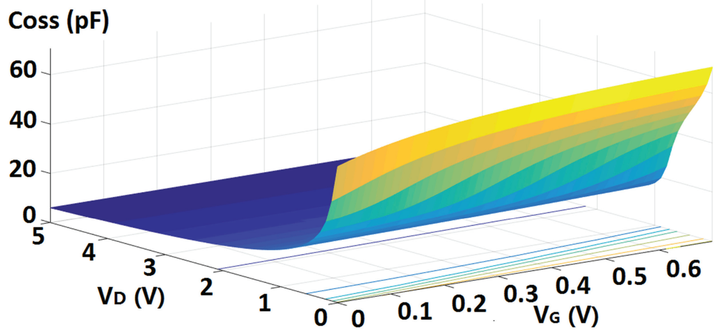


Figure 3. Nonlinearities of C_{oss} (off-state and the gate voltage is much lower than the threshold voltage)

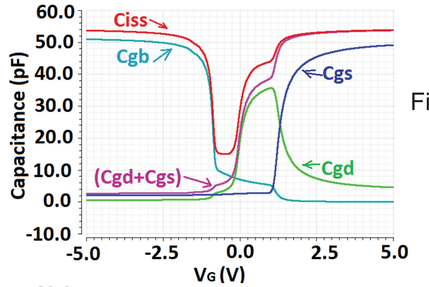


Figure 4. Nonlinear parasitic capacitances looking into the gate terminal ($V_D = V_B = V_S = 0$ V)

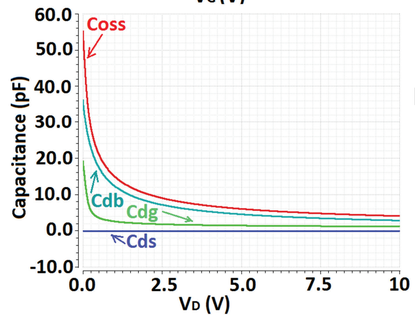


Figure 5. Nonlinear parasitic capacitances looking into the drain terminal (off-state, $V_G = V_B = V_S = 0$ V).

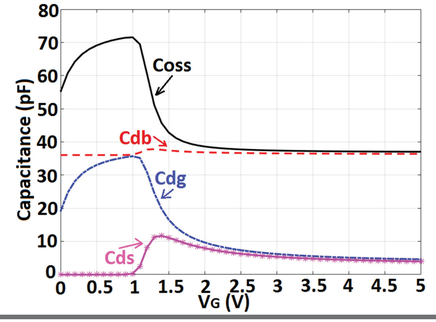


Figure 6. Nonlinear parasitic capacitances looking into the drain terminal (on-state in the linear region, or in the sub-threshold region, as well as off-state, $V_D = 1$ µV, $V_B = V_S = 0$ V).

Technical University of Denmark, Department of Electrical Engineering
Richard Petersens Plads 325, Room 258, 2800 Kgs. Lyngby, Denmark
Email: linfan@elektro.dtu.dk Phone: +45 4525 3481

Intrinsic Nonlinearities and Layout Impacts of 100 V Integrated Power MOSFETs in Partial SOI Process

Lin Fan, Arnold Knott, Ivan Harald Holger Jørgensen
Technical University of Denmark, Department of Electrical Engineering, Electronics Group
Richard Petersens Plads, Building 325, Room 258, 2800 Kgs. Lyngby, Denmark

Intrinsic Nonlinearities in Time-Domain

(Nonlinear Gate Charges and FOMs)

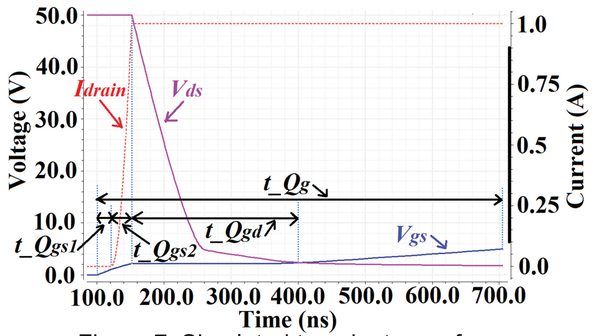


Figure 7. Simulated transient waveforms and naming conventions.

$$FOM_{com1} = R_{ds} \cdot Q_g \quad (1)$$

$$FOM_{com2} = R_{ds} \cdot Q_{gd} \quad (2)$$

$$FOM_{hard-sw} = R_{ds} \cdot (Q_{gd} + Q_{gs2}) \quad (3)$$

$$FOM_{soft-sw} = R_{ds} \cdot (Q_g + Q_{oss}) \quad (4)$$

Same as in Fig. 9	Best-case FOM vs. Worst-case FOM FOM is lowered: by times (by percentage)			
	FOM_{com1}	FOM_{com2}	$FOM_{hard-sw}$	$FOM_{soft-sw}$
V_{gs}	1.5 (32 %)	1.3 (22 %)	1.3 (22 %)	N/A
I_{drain}	2.2 (55 %)	3.0 (67 %)	3.7 (73 %)	N/A
V_{ds}	1.4 (30 %)	18.3 (95 %)	2.2 (54 %)	2.2 (54 %)

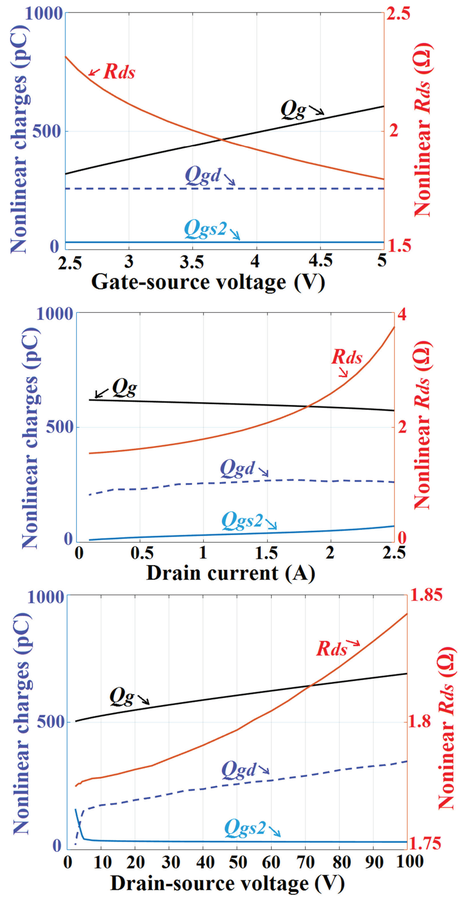


Figure 8. Gate charge Q_g, its sub-components Q_{gd} and Q_{gs2}, and final-state R_{ds} (simulated).
(a) Versus final-state V_{gs}
(b) Versus final-state I_{drain}
(c) Versus original-state V_{ds}

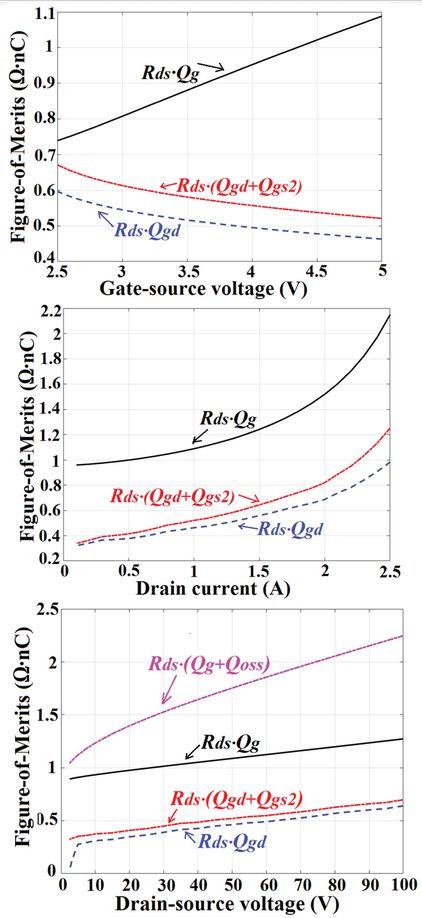


Figure 9. Nonlinear FOMs (simulated).
(a) Versus final-state V_{gs}.
(b) Versus final-state I_{drain}.
(c) Versus original-state V_{ds}.

Technical University of Denmark, Department of Electrical Engineering
Richard Petersens Plads 325, Room 258, 2800 Kgs. Lyngby, Denmark
Email: linfan@elektro.dtu.dk Phone: +45 4525 3481

Intrinsic Nonlinearities and Layout Impacts of 100 V Integrated Power MOSFETs in Partial SOI Process

Lin Fan, Arnold Knott, Ivan Harald Holger Jørgensen
Technical University of Denmark, Department of Electrical Engineering, Electronics Group
Richard Petersens Plads, Building 325, Room 258, 2800 Kgs. Lyngby, Denmark

Layout Structure Impacts

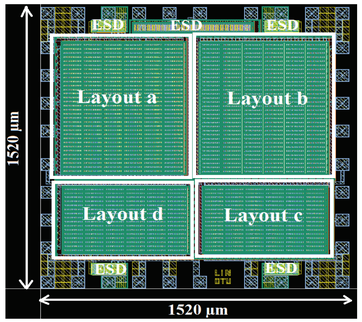
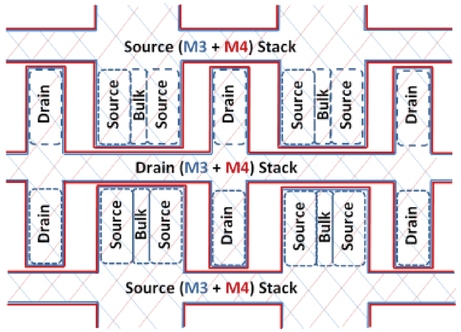


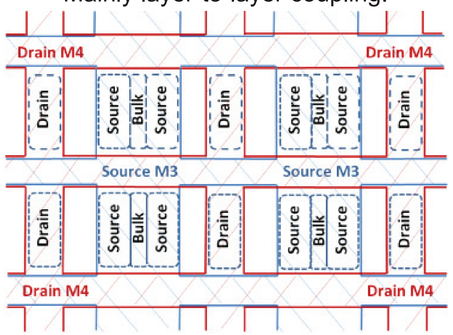
Figure 10. Layout of the chip design (proposed structures are highlighted)

R/C	Top chip-level (including chip-pads and ESD protections)					
	Schematic *a* & *b*	Post-Layout *a*	Post-Layout *b*	Schematic *c* & *d*	Post-Layout *c*	Post-Layout *d*
Parasitic	No	2D Extract	2D Extract	No	2D Extract	2D Extract
$R_{ds(on)}$ (Ω)[a]	1.542	2.071	2.250	3.085	3.354	3.295
$C_{g\text{-}sb}$ (pF)[b]	21.3	46.9	49.5	11.5	25.1	26.7
C_{gd} (pF)[b]	38.1	41.4	39.3	19.1	20.6	20.6
C_{iss} (pF)[b]	59.4	92.7	93.2	30.6	48.0	48.9
$C_{d\text{-}sb}$ (pF)[c]	72.1	88.4	85.7	36.0	47.6	48.0
C_{dg} (pF)[c]	38.1	41.4	39.3	19.1	20.6	20.6
C_{oss} (pF)[c]	110.2	132.1	127.6	55.1	69.5	69.8
$R_{ds(on)}\cdot C_{iss}$ (ps)	91.6	192.0	209.7	94.4	161.0	161.1
$R_{ds(on)}\cdot C_{oss}$ (ps)	169.9	273.6	287.1	170.0	233.1	230.0

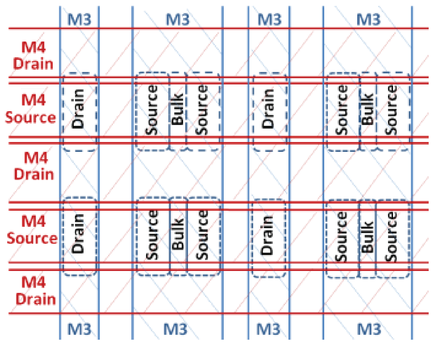
Layout *a*:
Drain/Source horizontal connection,
Mainly side-by-side coupling.



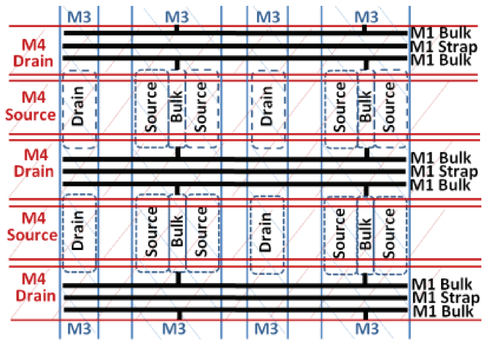
Layout *b*:
Drain/Source horizontal connection,
Mainly layer-to-layer coupling.



Layout *c*:
Drain/Souce vertical connection,
Perpendicular mesh structure



Layout *d*:
Drain/Souce structure the same as *c*
but Bulk as a seperate terminal.



Key Contributions

1) Systematically analyzed the nonlinear parasitic capacitances of integrated high voltage power MOSFETs in a partial SOI process.
2) A modeling method is proposed for analyses in different transistor states, whereas industrial datasheets typically specify only off-states.
3) Parasitic capacitances towards bulk can dominate over parasitic capacitances towards source.
4) The nonlinear FOMs are lowered by 1.3-18.3 times and improved by 22-95 % with optimized quasi-zero voltage switching conditions.
5) Parasitic capacitances of on-chip interconnections could dominate over intrinsic capacitances of power devices.
6) Side-by-side coupling dominated layout structures may perform better than layer-to-layer coupling dominated layout structures.

Acknowledgment:

This research was funded by a grant (No. 67-2014-1) for the TinyPower project from Innovationsfonden, Denmark.

References

[1] **L. Fan**, A. Knott, and I.H.H. Jørgensen, "Nonlinear parasitic capacitance modeling of high voltage power MOSFETs in partial SOI process," ISI-indexed Research Journal Elektronika ir Elektrotechnika, Vol. 22, No. 3, pp. 37-43, June 2016.
[2] **L. Fan**, A. Knott, and I.H.H. Jørgensen, "Layout capacitive coupling and structure impacts on integrated high voltage power MOSFETs," IEEE PRIME conference, June 2016.
[3] **L. Fan**, I.H.H. Jørgensen, and A. Knott, "Optimization of Nonlinear Figure-of-Merits of Integrated Power MOSFETs in Partial SOI Process," IEEE ET 2016 conference, September 2016.

Technical University of Denmark, Department of Electrical Engineering
Richard Petersens Plads 325, Room 258, 2800 Kgs. Lyngby, Denmark
Email: linfan@elektro.dtu.dk Phone: +45 4525 3481